LEARNING BASED DESIGN OF LOW POWER 2.5GHz PHASE LOCKED LOOP FOR COMMUNICATION USING 45nm TECHNOLOGY

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ABSTRACT

A well defined accurate tuning frequency oscillator is required in radio frequency application circuits and many analog circuits. The oscillator circuit integrated in a phase locked loop maintain a constant frequency and phase by using a external reference signal and which is compared with the operating frequency and phase. The external reference signal of phase locked loop (PLL) is tune the oscillator circuit for maintain the constant frequency and phase if any deviation happen in the comparison result. This paper describes the low power 2.5GHz range phase locked loop. The major parts of the phase locked loop are phase frequency detector, charge pump, voltage controlled oscillator and high speed divider. Layout design of phased locked loop with low power consumption is described in this paper. The PLL explained in this paper is implemented by 45nm CMOS technology. Low leakage high speed BSIM4 MOS transistor is used in the design. The main advantage of the 45nm CMOS technology is the metal gate and it has a gate oxide with high density and the dielectric of interconnect is very low. The layout of PLL is implemented by analog design tool microwind 3.1. The proposed layout of PLL is a modified design of oscillator circuit and divider circuit. The proposed architecture consumes only 13.482µW power with 0.4V supply voltage.

Keywords: Phase locked loop, Phase Detector, Charge Pump, Loop Filter, Voltage Controlled Oscillator, High Speed Divider, Microwind3.1, 45nm CMOS Technology

1. INTRODUCTION

Most of the recent electronic systems use the Phase Locked Loop (PLL) circuit. Timing jitter or phase noise of the PLL will reduce the performance of the systems which are designed by using PLL. Switching activities of MOS transistors introduce the substrate noise in such systems. The major problem in the modern circuit design is power consumption. Low power consumption is desired for designing of any system. PLL uses negative feedback which locks reference signal with feedback signal [1]. Clock and data recovery circuits, microprocessor clock generation and frequency synthesizer circuits uses the PLL [2]. The phase of the reference signal is matched with the phase of the feedback signals at lock mode. The PLL maintain the output is constant at lock mode by compare the two signals [3]. The reference signal is given to PLL by external timing circuit. Frequency

variations will appear due to changes in temperature, changes in supply voltage, aging of components and radiated emissions. Phase locked loops are required to design accurately in two circuits track named as frequency and phase. Hence only they communicate with each other reliably. Frequency tuning circuits uses the phase locked loop [4]. Power consumption is the one of the most important factor of design aspect for multi giga hertz communication systems such as optical communication, wireless communication, microprocessor and ASIC/SOC designs. Various domains such as communication and instrumentation uses PLL for different purposes. Frequency relation between two independent signal sources maintain a constant phase in phase locked loop [5].

This paper describes the design concepts for layout design of high speed performance and highly stable PLL with low power consumption using CMOS VLSI technology. The proposed PLL is a negative feedback system consists of five blocks such as phase detector, charge pump, loop filter, high performance voltage controlled oscillator (VCO) and high speed Frequency divider. This research work describes the design of low Power and high speed phase locked loop highly efficient layout with the use of CMOS VLSI technology. The design process usually have a gradual development nature at various design levels. The design process is starts with a requirements and desired output. The design has to be improved when the requirements are not meet the desired performance. The VLSI technology design steps consists of representation of expectations at output, path to reach the expectations, designing of logic circuits based on the path defined, conversion of logic circuits to CMOS circuits and physical layout [6]. The technique behind the circuit realization is the translinear characteristics of MOS transistors operating in the weak inversion mode [15].

The proposed PLL uses Microwind 3.1 VLSI Backend software for implement the layout. The physical description level of the proposed PLL is designed and simulated by this software. The 45 mm CMOS/VLSI technology is used for design the proposed PLL which offers high speed performance at low power. The best way to reduce consumption of power in the low power circuits and systems is reducing supply voltage [5]. Noise present on power supply affects the analog circuit performance when reducing the supply voltage with the technology. Voltage controlled oscillator (VCO) output frequency and charge pump control voltage are directly proportional to the noise on power supply.

2. METHODOLOGY

Wireless data are transmitted by using the RF signals. The Digital Signal Processing technology uses the RF signals for transmit data. Wireless transceivers must have the ability to produce RF signals with wide range of frequencies. This is upconvert the data for transmission and downconvert the received signal for processing. In an communication systems, for clock and data recovery applications monolithic phase locked loops are used. For wireless application, monolithic phase locked loops are used as a clock generator and distributor in microprocessor and frequency synthesizer [7]. A proposed PLL is a positive feedback system which consists of five blocks. They are: phase detector, charge

pump, loop filter, high performance voltage controlled oscillator (VCO) and a high speed frequency divider.

The microwind 3.1 convert the CMOS circuit of each block logic circuit into Physical layout using lambda based rules. Overall layout is obtained by cascading the layout of each block. This research mainly focus on the analysis and design of low power consumption and high speed performance phase locked loop using VLSI technology.

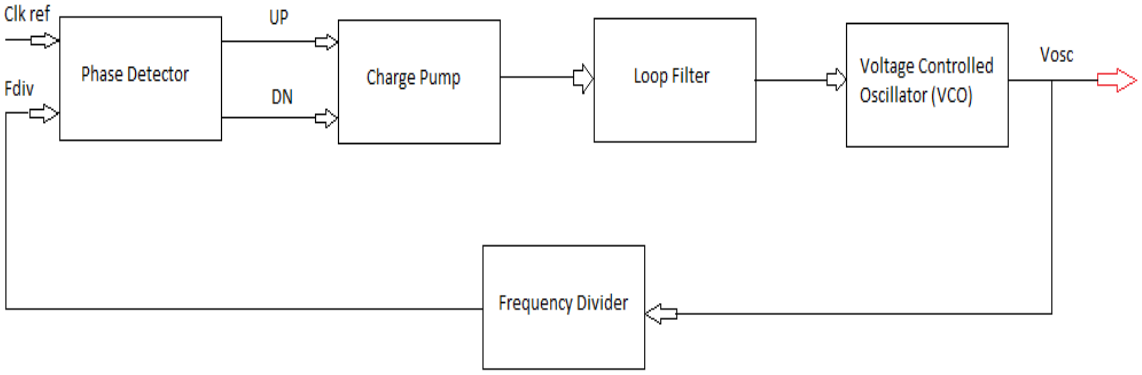

Figure 1 : Proposed Architecture of PLL

2.a. PHASE DETECTOR

The phase difference between the operating frequency of PLL and reference signal is determined by the phase detector. The output of the phase detector is proportional to the phase difference. The output signal of the phase detector is used to maintain the output of the VCO as constant and it align the two outputs through a feedback network. There are two inputs in phase detector. The first input is a clock reference signal which is obtained from external circuit and the second input is the output of the high speed frequency divider. Phase detectors are two types. They are XOR phase detector and phase frequency detector.

XOR phase detector may lock to the multiple of the clock frequency. Upto the 50% of duty cycle, the output of the phase detector is square wave when the local clock is a multiple of the reference clock frequency and albeit at a different frequency. This is the disadvantage of XOR phase detector.

The drawback of the XOR phase detector is solved by phase frequency detector (PFD) and which is mostly used in the PLL circuit. The PFD output depend on the phase and frequency difference of the inputs given and there is no possibility to lock an incorrect multiple of the frequency. The PFD uses two clock inputs named as Clkref and Fdiv and produces two outputs named as UP and DN [6].

$$V_{in} = E_{in}\sin(wt)$$

$$V_{div} = E_{div}\sin(\omega t - \varphi_d + 90^0) = E_{div}\cos(\omega t - \varphi_d)$$

Where, V_{in} and V_{div} are the input reference signal and divider signal repectively.

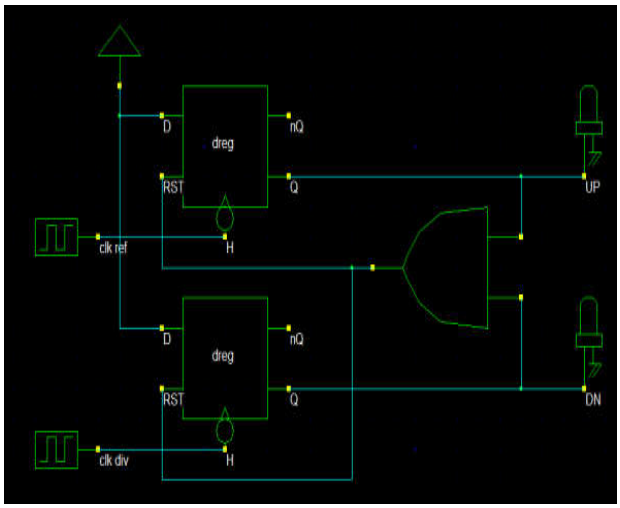

Figure 2 : Phase Frequency Detector

2.b. CHARGE PUMP

The charge pump has three states. The states are Sink Current, Source current and Tri state (High Impedance). The charge pump is in source current state when the output frequency or phase is too low. The charge pump is in sink current state when the output frequency or phase is too high. The charge pump is in high impedance state when the output frequency or phase is correct. Theoretically, the charge pump may sink and source the same current, but in practically not sink and source the same current. Since, some mismatch between sink and source current. This mismatch is undesirable. Since, it can cause reference spurs and affect lock time [6].

The charge pump converts logic states of PFD output into analog signal making it suitable to control VCO frequency. Current will flow out of charge pump and charges loop filter when PFD output is high. The UP signal add the charges proportional to the size of the UP signal and the DN signal removes the charges proportional to the size of the DN signal [6]. A net increase in the control voltage when width of the UP signal is greater than the width of the DN signal.

$$V_{out} = K_M \frac{E_{in} E_{div}}{2} [sin(\varphi_d) + sin(2\omega t - \varphi_d)]$$

Where, K_M is the multiplication constant of phase detector.

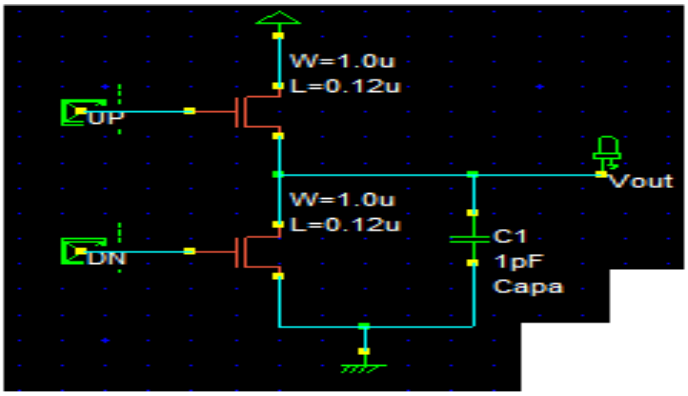

Figure 3 : Charge Pump

2.c. LOOP FILTER

Low pass filter act as a loop filter. The integrator with some addition of components act as a loop filter. The PLL performance, switching time, Bandwidth and Reference spurs of the PLL is calculated by loop filter. It smoothen the control output from the charge pump. The oscillator away from the reference frequency at initially. Phase detectors have the capability of respond to this frequency difference situation. Increasing the lock in range is must for allowable inputs [6]. The low pass filter for proposed PLL is designed using virtual resistance of 1kΩ with capacitor of 2pf.

$$V_c = K_{IF} K_M \frac{E_{in} E_{div}}{2} \varphi_d$$

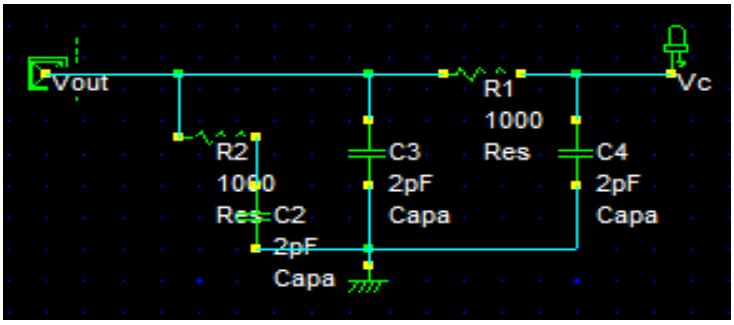

Figure 4 : Schematic of Loop Filter

2.d. VOLTAGE CONTROLLED OSCILLATOR

The voltage controlled oscillator is the most important block in PLL in terms of noise contribution. The three stage ring oscillator was chosen to obtain the necessary output frequency range at low power consumption. To minimize the flicker noise contribution the channel length of NMOS and PMOS in delay cell was chosen to be 25nm. The V-I converter was implemented using a simple source degenerated transistor stage. To improve the linearity of the VCO , a current split control technique was utilized. The VCO buffer was designed with a low threshold inverter to accommodate the swing variation in the VCO. Since the duty cycle does not play any role in this architecture, the skewed inverter buffer provides a simple solution to the buffer stage of the VCO. The VCO was designed considering the random and deterministic jitter requirement.

$$\varphi(s) = \frac{\omega(s)}{S}$$

Where, φ(s) and ω(s) are the Laplace transform of VCO instantaneous phase and frequency. This equation relates the input control voltage and phase of output signal of VCO.

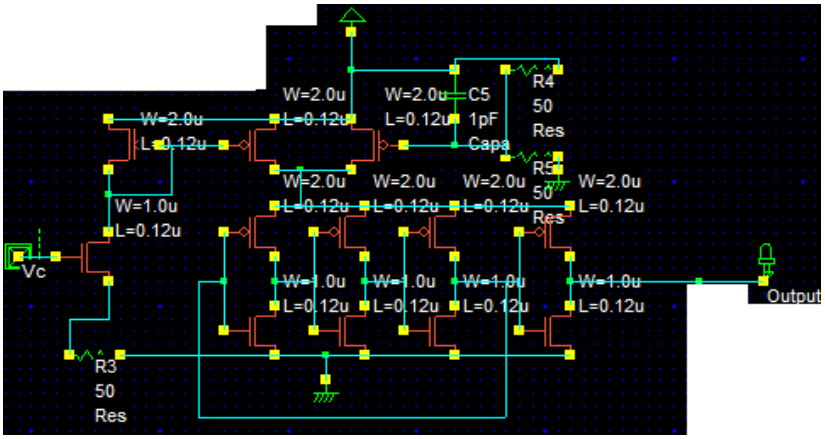

Figure 5 : Schematic of VCO

2.e. FREQUENCY DIVIDER

The frequency divider in the PLL is a high speed building block. True single phase divider was chosen for high speed and dynamic power consumption. Edge triggered D – Flip Flop circuit in giga hertz single phase clock optimize the speed.

$$\varphi_{div}(s) = \frac{\varphi(s)}{N}$$

Where, N is the division ration of divider circuit.

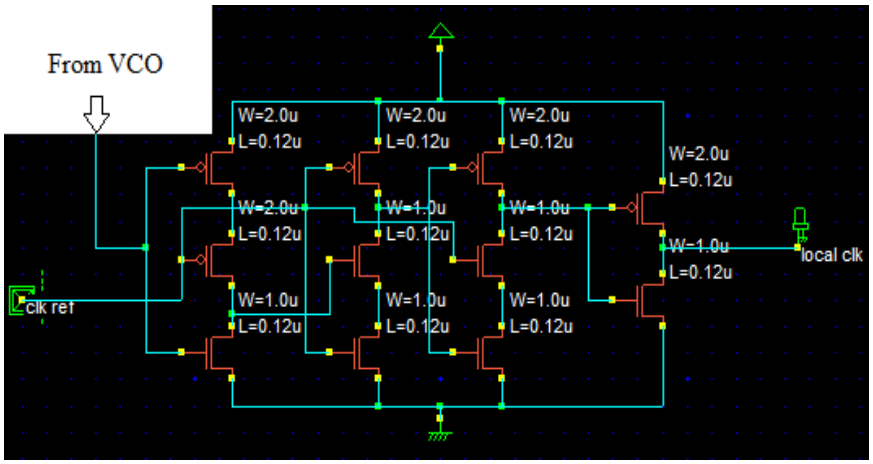

Figure 6 : Schematic of Frequency Divider

2.f. LAYOUT OF PROPOSED PLL

45 nm design rule is used for design the layout of this PLL with the aid of microwind 3.1 software. The supply voltage used in this design is 0.4V. This PLL is designed for 2.5GHz frequency. Low leakage BSIM4 transistors are used for low power. The power consumption at 2.54GHz frequency is 13.482µwatts.

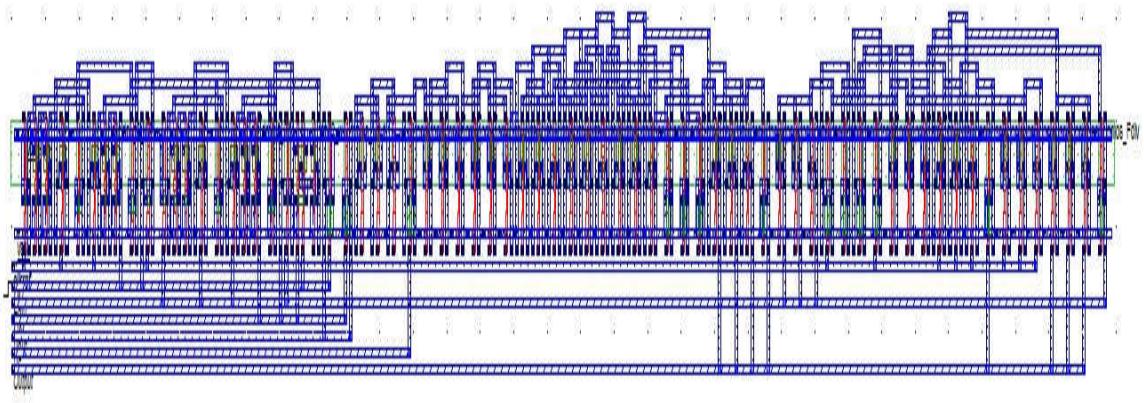

Figure 7 : Layout of proposed PLL

3. EXPERIMENTAL RESULT AND DISCUSSION

This paper describes the improvement of low power consumption of PLL by using CMOS 45nm technology and it is implemented by Microwind 3.1. The metal gate length is 25nm and SiON gate dielectric is used. The analysis of designed PLL shown the low power consumption, low power dissipation and stability of frequency in the scale of voltage level. The below table shows the comparison of power consumption of different CMOS technologies with step size 1ps.

Table 1
Comparison of power consumption

Technology	**Voltage Level**	**Power Consumption**
0.6µm	5V	19.956mW
0.8µm	5V	18.019mW
0.12µm	1.2	0.854mW
0.18µm	2V	2.333mW
0.25µm	2.5V	4.232mW
0.35µm	3.5V	5.557mW
1.2µm	5V	18.862mW
45nm	**0.4V**	**13.482µW**
65nm	0.7V	0.143mW
90nm	1.2V	1.172mW

The below table shows the comparison of power dissipation of different CMOS technologies.

Table 2

Comparison of power dissipation

Technology	**Voltage Level**	**Power Dissipation**
0.6µm	5V	19.953mW
0.8µm	5V	18.019mW
0.12µm	1.2V	0.854mW

0.18µm	2V	2.333mW
0.25µm	2.5V	4.033mW
0.35µm	3.5V	5.557mW
1.2µm	5V	18.865mW
45nm	**0.4V**	**0.013mW**
65nm	0.7V	0.125mW
90nm	1.2V	1.172mW

The below table shows the data array of Vdd with respect to the frequency. It clearly shows that the frequency is remains stable upto 0.4V and there is a large change in frequency when the supply voltage rises above 0.4V.

Table 3

Frequency variation with supply voltage

SI. No.	**Vdd**	**Frequency (GHz)**
1.	**0.1**	**2.545**
2.	**0.2**	**2.545**
3.	**0.3**	**2.545**
4.	**0.4**	**2.545**
5.	0.5	6.993
6.	0.6	11.494
7.	0.7	15.625
8.	0.8	18.182

The below graphical representation shows the variation of Vdd with respect to the frequency.

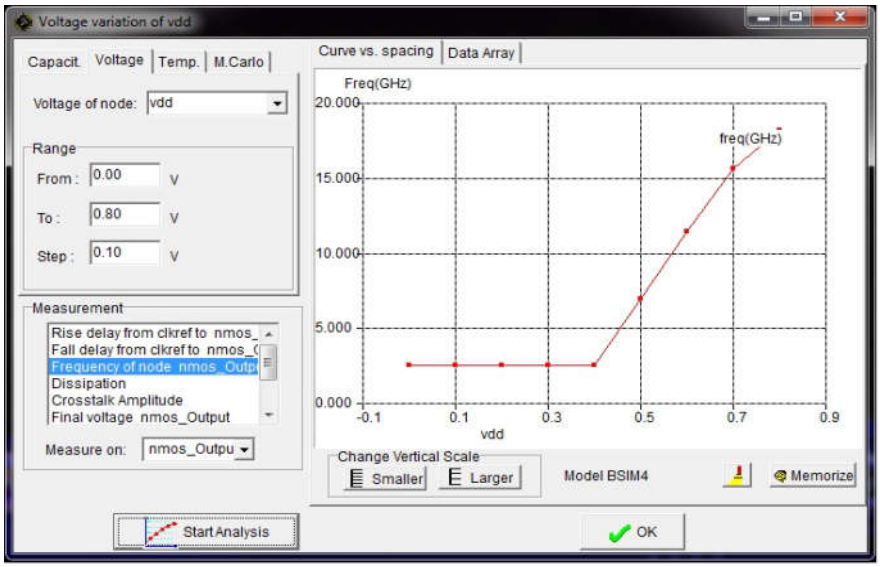

Figure 8 : Frequency variation with Vdd

The below graphical representation shows the frequency response of the designed PLL.

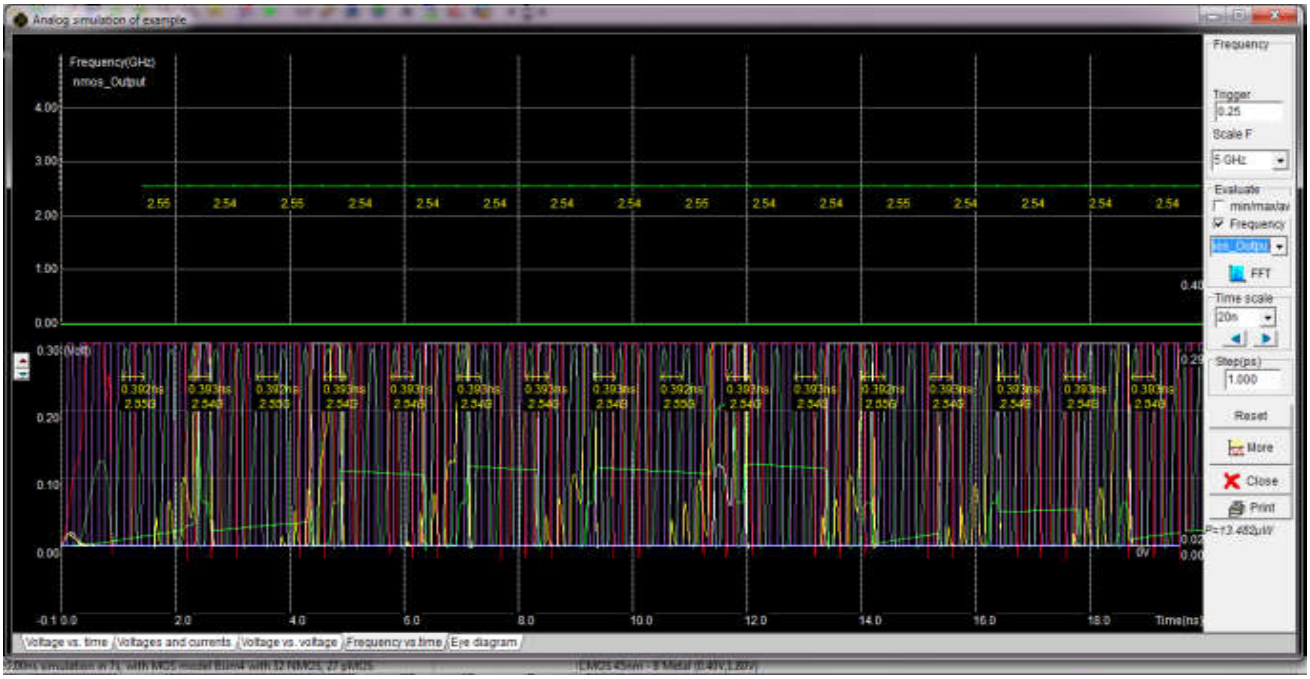

Figure 9 : Frequency response

4. CONCLUSION

The first three blocks are not changed which are similar to the existing PLL. The proposed PLL layout is a modified design of VCO and divider for achieving low power and high speed performance. The proposed PLL is highly stable. Since, the supply voltage V_{dd} from 0.0V to 0.8V is varied and it is analyzed against frequency. It is found that the proposed PLL is stable upto the designed voltage level which proves the high stability of the PLL. The power consumption of proposed PLL is very low. The power dissipation measured from the parametric analysis of design tool, by V_{dd} at 0.4V is 0.013 microwatt range which shows the power consumption is very low. A 2.5GHz High efficient, low power and optimum area PLL is designed in this proposed method. The proposed architecture consumes only 13.482µW power with 0.4V supply voltage**.** The switching performance of MOS transistor in 45nm CMOS technology is increased to 30% when compared to 65nm CMOS technology which proves the high speed performance of the PLL.

5. FUTURE WORK

The proposed PLL output frequency at 0.4 supply voltage is 2.45GHz. The output frequency is increased when the supply voltage is increased. But, the power consumption is increased. This work can be extended for high frequency range by modified design of flip flops used in VCO and divider circuits in the same technology at same supply voltage level. Also, this work can be implement in 32nm CMOS technology which consumes low power. But, the crosstalk effect is a considerable factor in this technology.

CONFLICT OF INTEREST

There is no conflict of interest in this research work.

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